The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A programmable logic device (PLD) including a plurality of logic array blocks (LAB's) connected by a PLD routing architecture, wherein at least one LAB is configured to determine a compression of a plurality of N-bit numbers, the one LAB comprising:

a plurality of look-up table (LUT) logic cells, each look-up table (LUT) logic cell configured to input three **operand** signals at three respective inputs of that look-up table (LUT) logic cell and to output two signals at two respective outputs of that look-up table logic cell (LUT) that are a sum and carry signal resulting from adding the three **operand** input signals;

input lines configured to receive input signals from the PLD routing architecture that represent the plurality of N-bit numbers and output lines configured to provide output signals to the PLD routing architecture that represent the compression of the plurality of N-bit numbers; and

LAB internal routing logic, not part of the routing architecture of the PLD, connecting the LUT logic cells such that the LUT logic cells collectively process the input signals, received at the input lines, that represent the N-bit numbers to generate the output signals, provided at the output lines, that represent the sum of the N-bit numbers.

2. (Original) The PLD of claim 1, wherein:

the LUT logic cells are organized into slices, each slice performing processing relating to a separate one of the bits of the N-bit numbers.

3. (Original) The PLD of claim 1, wherein:

each of the input lines is configured to receive one bit of one of the N-bit numbers.

4. (Original) The PLD of claim 1, wherein:

at least some of the input lines are configured to receive more than one bit of the plurality of N-bit numbers.

5. (Cancelled)